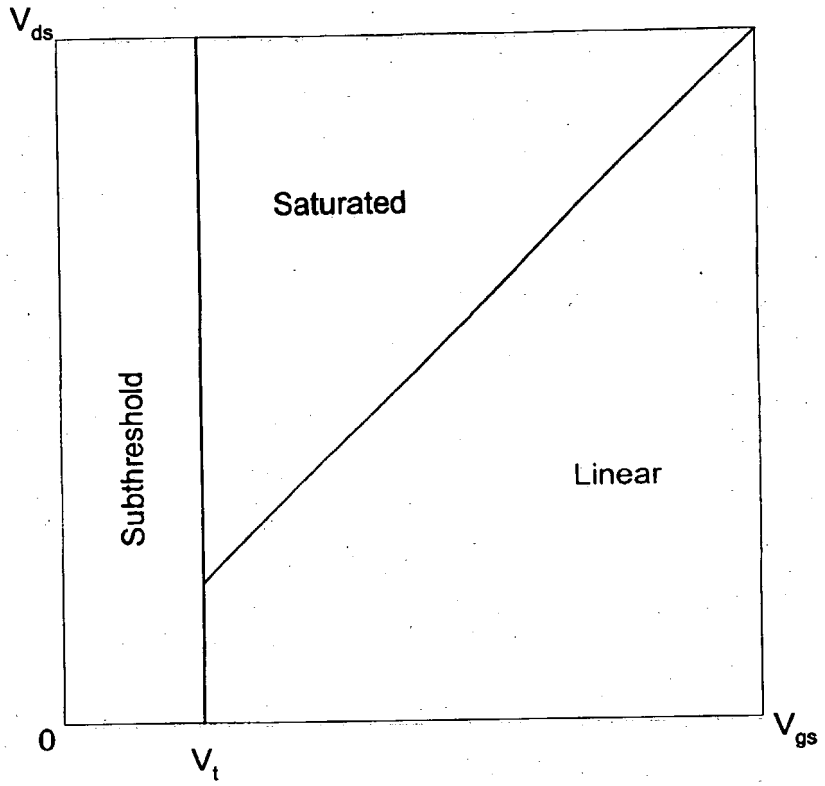
FIG. 1


V_{ds}
Saturated
Subthreshold
Linear
0
V_t
V_{gs}

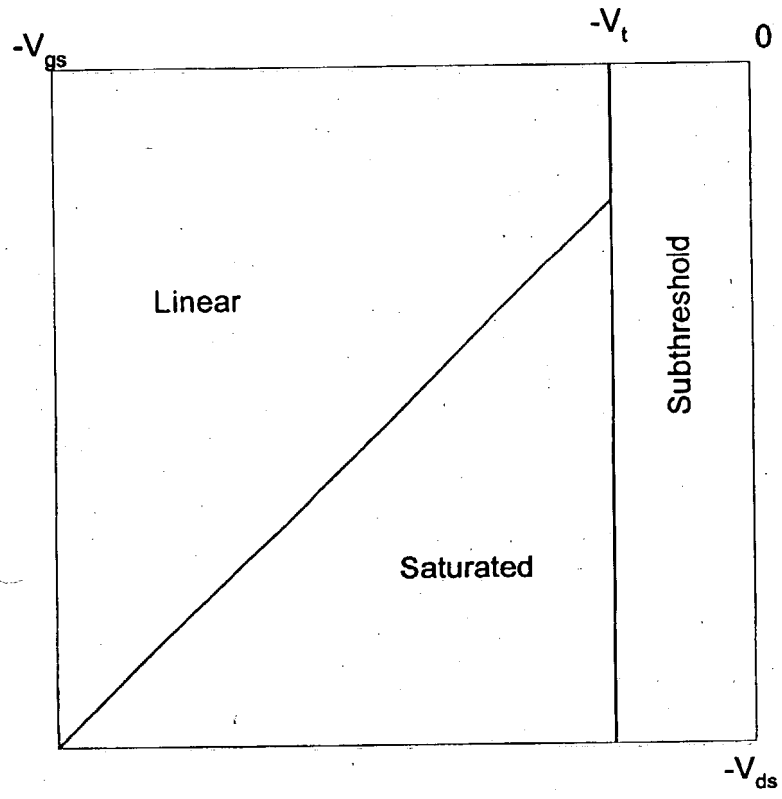
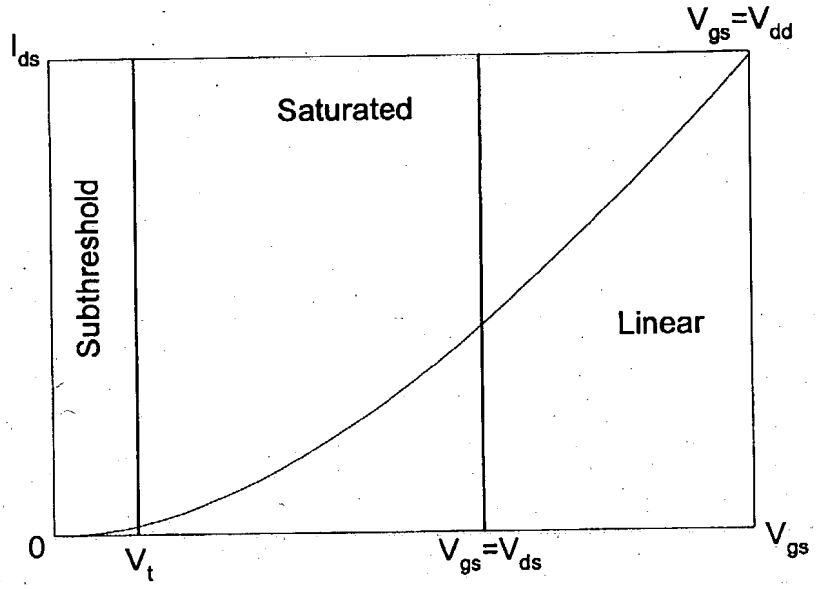

$-V_{gs}$
$-V_t$
0
Linear
Subthreshold
Saturated
$-V_{ds}$

FIG. 2

FIG. 3


I_{ds}
$V_{gs}=V_{dd}$
Saturated
Subthreshold
Linear
0
V_t
$V_{gs}=V_{ds}$
V_{gs}

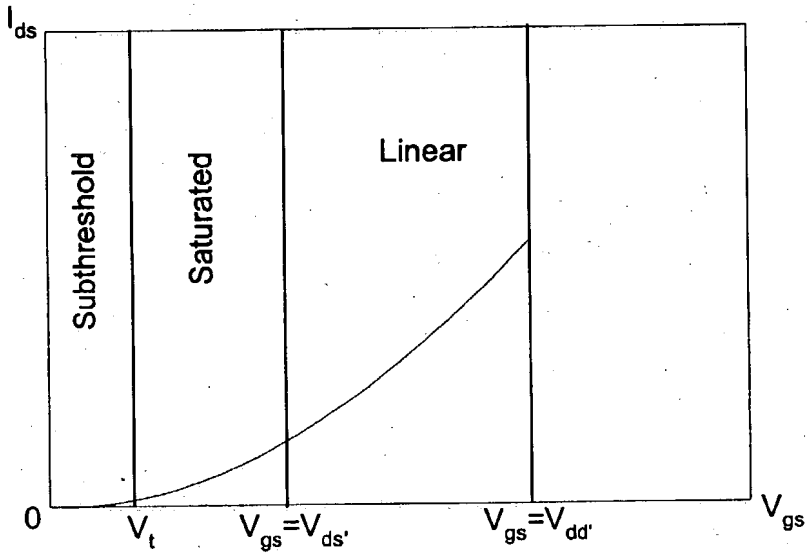

I_{ds}
Subthreshold
Saturated
Linear
0
V_t
$V_{gs}=V_{ds'}$
$V_{gs}=V_{dd'}$
V_{gs}

FIG. 4

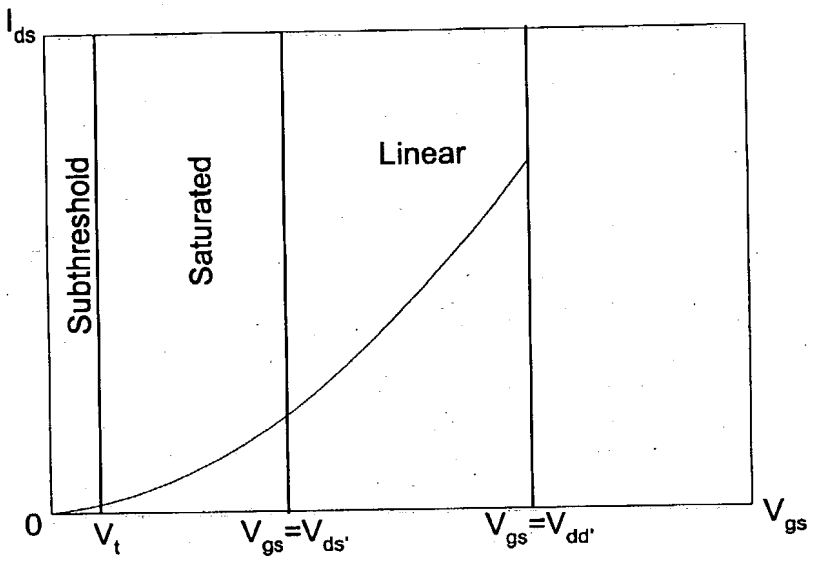
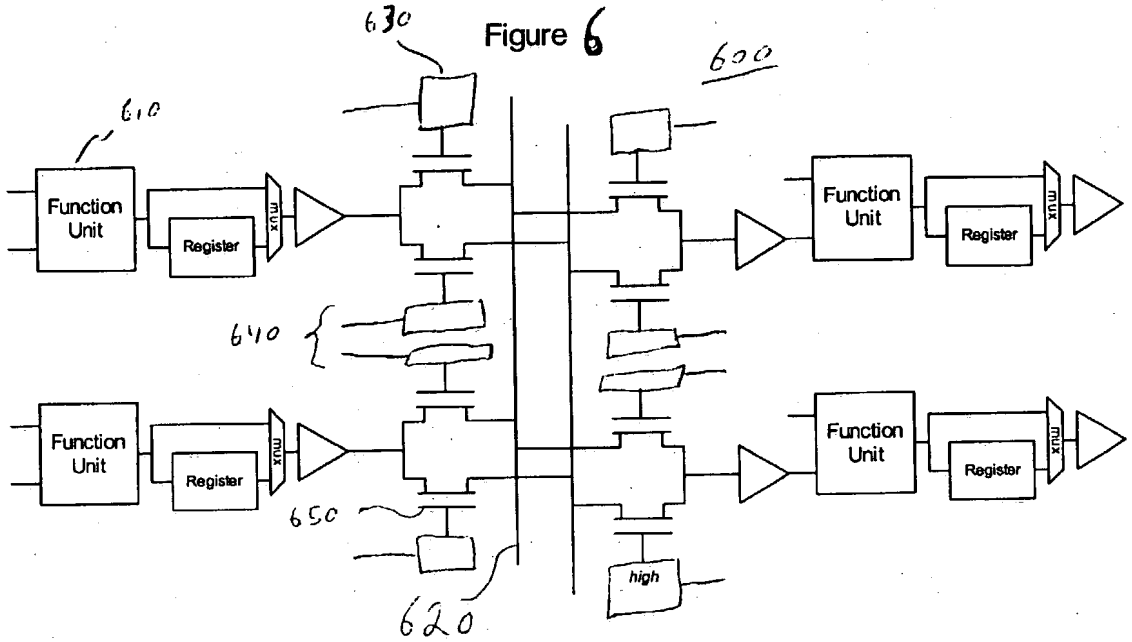


FIG. 5

Figure 6



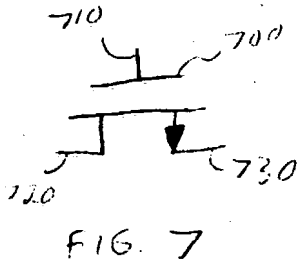


FIG. 7

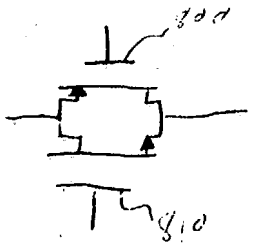
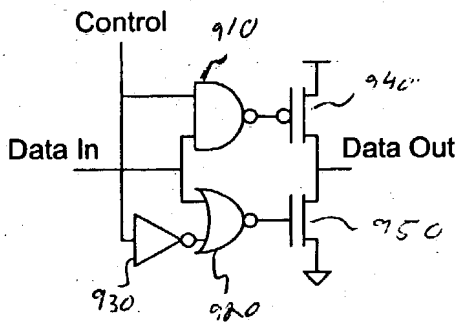


FIG. 8

Controlled buffer

FIG. 9



Tristate buffer

FIG. 16A

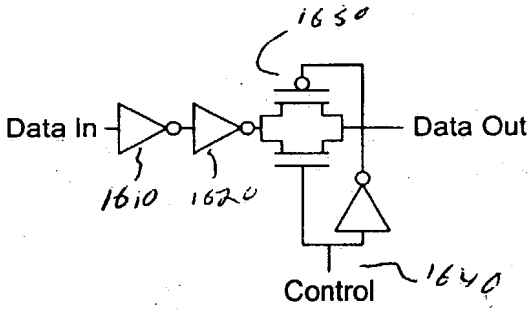


FIG. 16B

Barrel Shifter

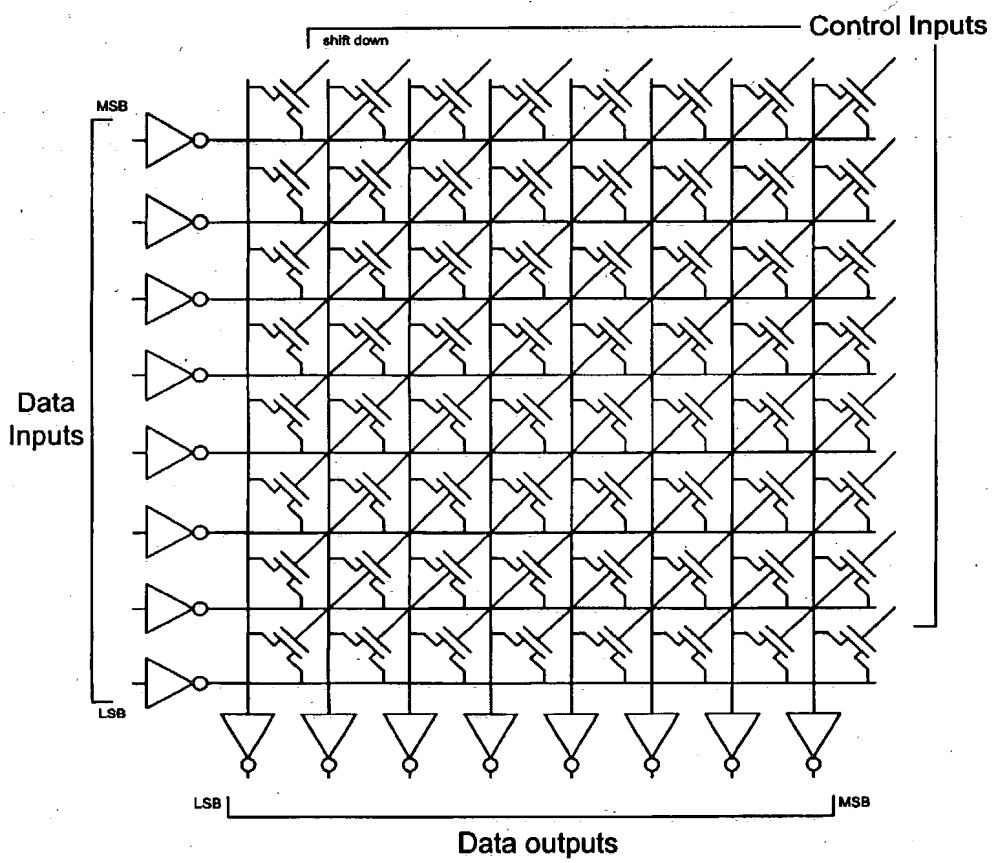
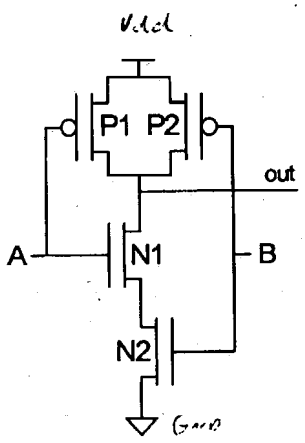
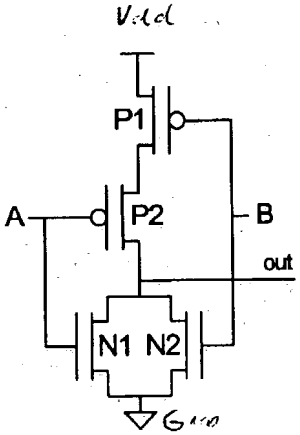


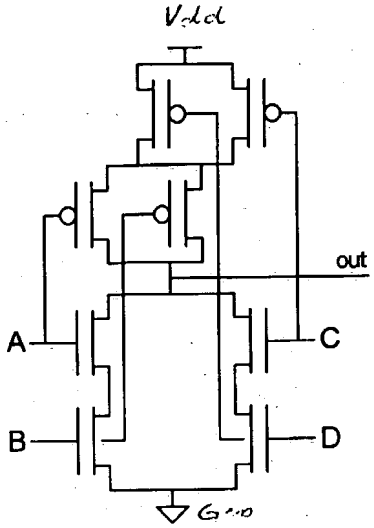
Figure 10



a) NAND gate



b) NOR gate



c) AND-OR-Invert gate
out = not (A.B | C.D)

Figure 11

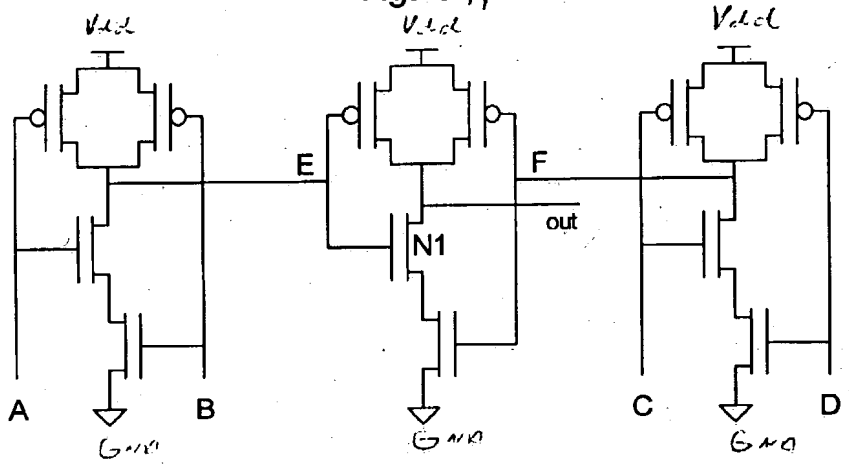


FIG. 12

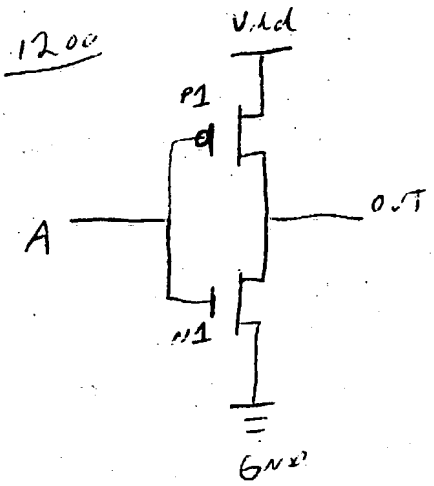


Figure 13

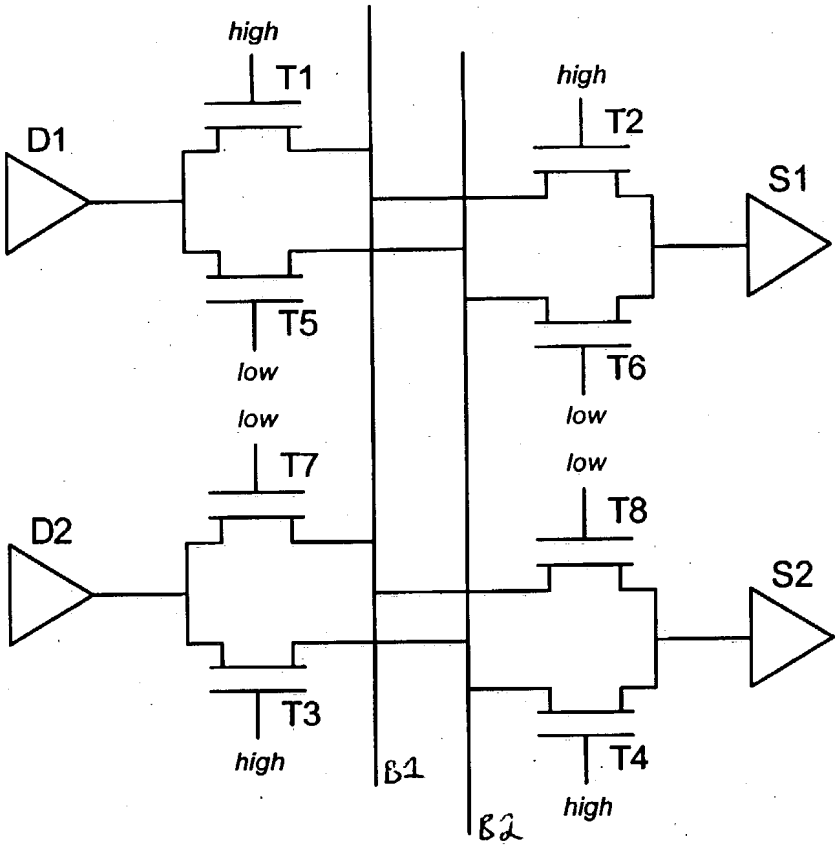

high
T1
high
T2
D1
S1
T5
low
T6
low
low
T7
low
T8
D2
S2
T3
high
B1
T4
high
B2

Figure 14

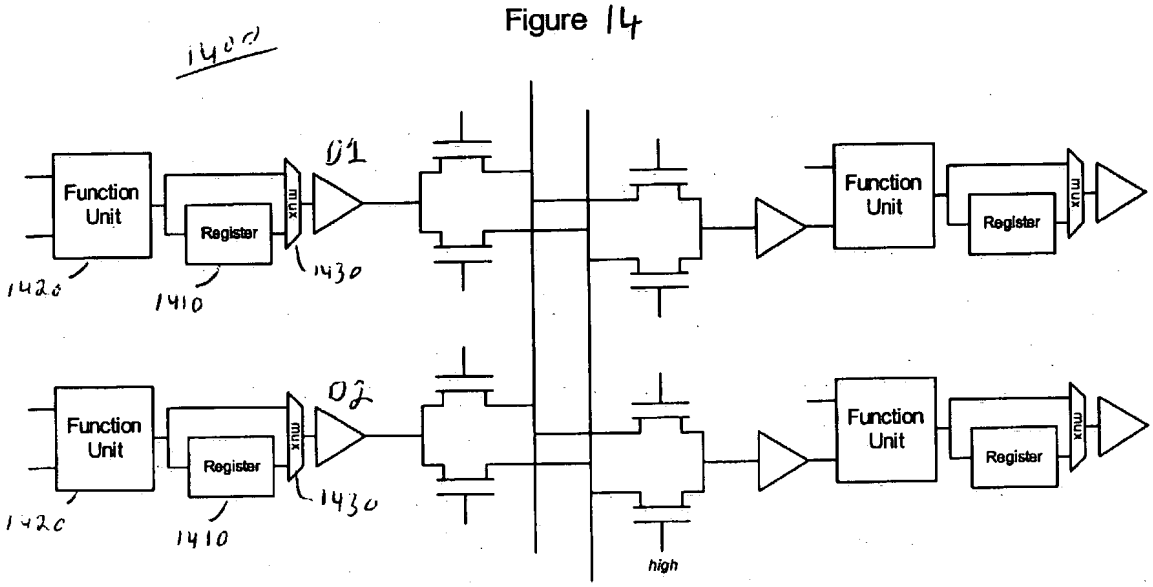
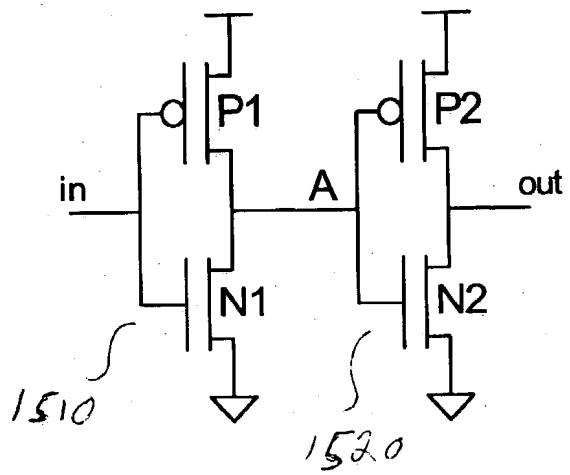

1400
Function Unit
Register
mux
Φ1
1420
1410
1430
Function Unit
Register
mux
Function Unit
Register
mux
Φ2
1420
1410
1430
high

Figure 15



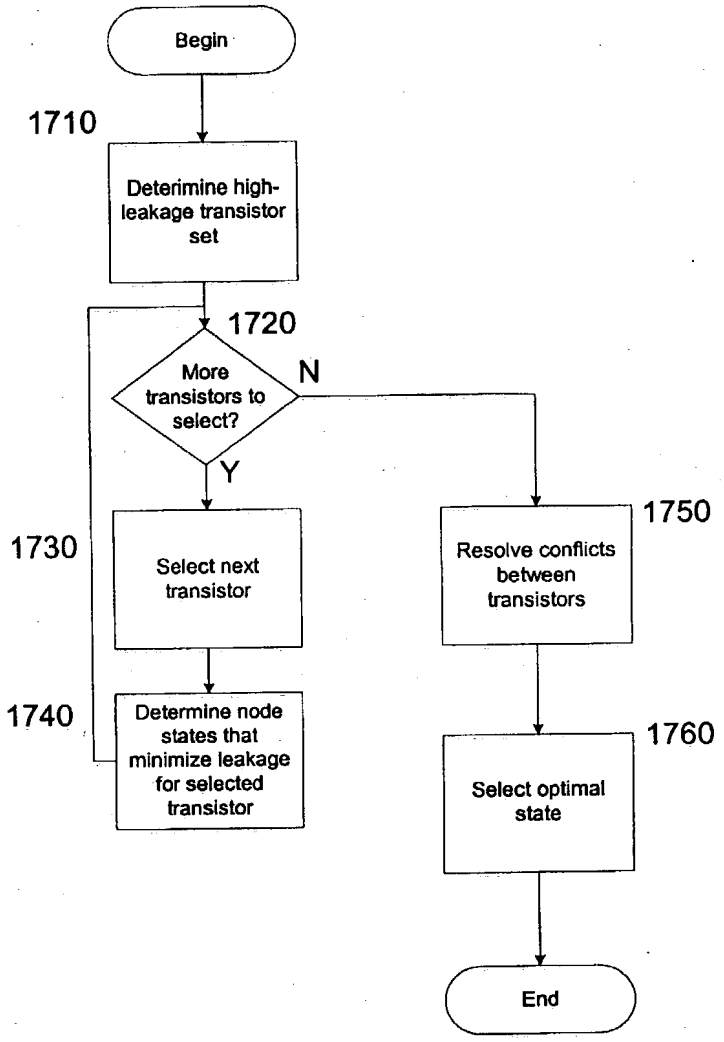

Begin
1710
Deterimine high-leakage transistor set
1720
More transistors to select?
N
Y
1730
Select next transistor
1740
Determine node states that minimize leakage for selected transistor
1750
Resolve conflicts between transistors
1760
Select optimal state
End

FIG. 17

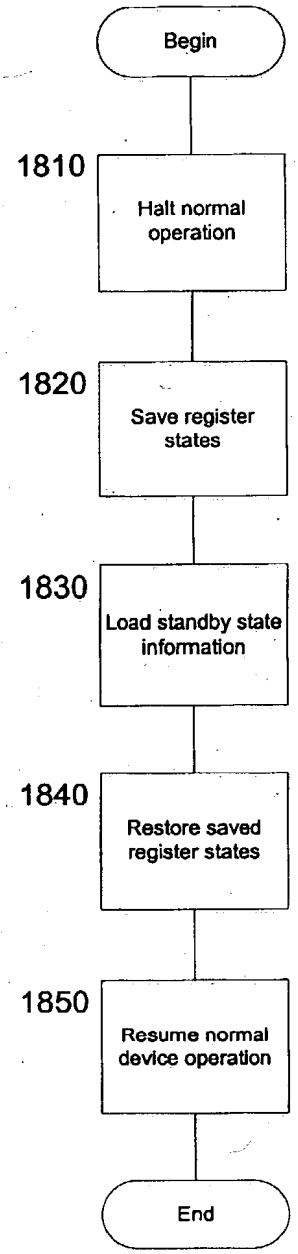

Begin
1810
Halt normal operation
1820
Save register states
1830
Load standby state information
1840
Restore saved register states
1850
Resume normal device operation
End

FIG. 18